IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS

Appellants:	Frankie F. Roohparvar Kevin Widmer
Serial No.	09/943,399
Filing Date	August 30, 2001
Group Art Unit	2818
Examiner	Ly D. Pham
Confirmation No.	8233
Attorney Docket No.	400.130US01

APPEAL BRIEF

Title: FLASH MEMORY WITH RDRAM INTERFACE

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1. Introduction

On July 31, 2003, Appellant filed a notice of appeal from the final rejection of claims 1 – 4 and 14 – 19 as set forth in the Final Office Action mailed June 25, 2003. Three copies of this Appeal Brief are hereby timely filed on September 8, 2003, and are accompanied by a fee in the amount of $320.00 as required under 37 C.F.R. §1.17(c).

2. Real Party in Interest

The real party in interest in the above-captioned application is the assignee Micron Technology, Inc.

3. Related Appeals and Interferences

There are no other appeals or interferences known to Appellant that will have a bearing on the Board's decision in the present appeal.

4. Status of the Claims

Claims 1 – 4 and 14 – 19 are pending in the application and are the subject of this appeal. In the Final Office Action mailed June 25, 2003, claims 1 – 4 and 14 – 19 were rejected under 35 U.S.C.§103(a). See Appendix A for the pending claim set.

5. Summary of the Amendments

This application was originally filed on August 30, 2001 with claims 1 – 13. The Examiner issued a restriction requirement that was mailed September 18, 2002. Appellant responded by electing claims 1 – 4, canceling claims 5 – 13 and adding new claims 14 – 19 in a

response mailed October 18, 2002. Claims 1 – 4 and 14 – 19 were rejected in a non-final office action mailed December 19, 2002. Appellant responded to the non-final office action with a response mailed February 5, 2003. Claims 1 – 4 and 14 – 19 were rejected in a final office action mailed April 2, 2003. Appellant responded with an amendment after final mailed April 30, 2003 amending claims 1, 4, and 18. The Examiner responded with an advisory action, mailed May 15, 2003, stating the amendment would not be entered due to new issues being raised. A request for continued examination was mailed May 30, 2003. A final office action was mailed June 25, 2003 rejecting claims 1 – 4 and 14 – 19. An amendment after final was not filed. Claims 1 – 4 and 14 – 19 are thus pending and the subject of this appeal.

6. Summary of the Invention

The present invention encompasses a flash memory device that is Rambus Dynamic Random Access Memory (RDRAM) compatible. Figure 2 and page 5, paragraphs 18 and 19 and page 6, paragraph 22 show and describe a flash memory device that has an interconnect configuration that is substantially similar to RDRAM packages. This enables both non-volatile and volatile memory devices to use the same memory bus. Additionally, both types of memories can respond to common command signals although the command signals may be interpreted differently by the memories.

7. Issues Presented for Review

The question presented in this appeal is whether the Examiner erred in rejecting claims 1 – 4, 14 – 15, and 18 under 35 U.S.C. §103(a) as being unpatentable over *Chen et al.* (US Patent No. 6,324,602) and claims 16, 17, and 19 under 35 U.S.C. §103(a) as being unpatentable over *Chen et al.* in view of *Deneroff et al.* (US Patent No. 6,215,686).

8. Grouping of Claims

Each of claims 1 – 4 and 14 – 19 stand or fall on their own merits for the reasons detailed below. Each of these claims is patentably distinct under 35 U.S.C. §103(a), as explained herein.

9. Argument

A. The Applicable Law

35 U.S.C.§103 provides in relevant part:

Conditions for patentability; non-obvious subject matter.

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

"The ultimate determination ... whether an invention is or is not obvious is a legal conclusion based on underlying factual inquiries including: (1) the scope and content of the prior art; (2) the level of ordinary skill in the prior art; (3) the differences between the claimed invention and the prior art; and (4) objective evidence of nonobviousness." *In re Dembiczak*, 175 F.3d 994, 998, 50 USPQ2d 1614, 1616 (1999) (citing *Graham v. John Deere Co.*, 383 U.S. 1, 17-18, 148 USPQ 459, 467 (1966)).

When applying 35 U.S.C. §103, the claimed invention must be considered as a whole; the references must be considered as a whole and must suggest the desirability and thus the obviousness of making the combination; the references must be viewed without the benefit of impermissible hindsight vision afforded by the claimed invention and a reasonable expectation of success is the standard with which obviousness is determined. *Hodosh v. Block Drug Co., Inc.*, 786 F.2d 1136, 1143 n.5, 229 USPQ 182, 187 n.5 (Fed. Cir. 1986).

To establish a prima facie case of obviousness, three basic criteria must be met: (1) There must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings; (2) There must be a reasonable expectation of success; (3) The prior art references must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in

the prior art, and not based on appellants' disclosure. *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991).

B. Scope and Content of Prior Art

Deneroff et al. discloses a memory system that includes switches for controlling data transfer. The Examiner included *Deneroff et al.* in the final office action only for its disclosure of the burst oriented read access operation relating to dependent claims 16, 17, and 19. Therefore, a detailed analysis of *Deneroff et al.* is neither necessary nor provided.

Chen et al. discloses an input/output interface for an integrated circuit device. Column 1, line 35 – col. 2, line 17 of *Chen et al.* discloses a listing of various RAM devices that incorporate previously developed interfaces. Within these paragraphs is a paragraph regarding a Rambus proprietary I/O interface as applied to a DRAM (i.e., column 1, line 66 – column 2, line9). Column 1, line 21 and column 4, line 51 of *Chen et al.* mention a flash memory device as being a typical memory device. *Chen et al.* does not disclose a flash memory device having a Rambus proprietary interconnect configuration.

The remainder of *Chen et al.* describes an input/output interface that uses a two-level protocol with bit compression and double data rate data transfer. As is stated in multiple locations of *Chen et al.*, the input/output interface allows for high speed/bandwidth memory accesses while reducing the pin count and operating frequency of a memory IC. According to *Chen et al.* this minimizes the package pin count and, therefore, the EMI on the PC board for high bandwidth memory applications. These advantages are discussed in the Abstract and column 3, lines 49 – 52, 56 – 61.

C. Analysis of Prior Art in Relation to Appellant's Claimed Invention

The Examiner finally rejected claims 1 – 4, 14 – 15, and 18 under 35 U.S.C. §103(a) as being unpatentable over *Chen et al.* Claims 16, 17, and 19 were rejected under 35 U.S.C. §103(a) as being unpatentable over *Chen et al.* in view of *Deneroff et al.*

The Examiner stated that *Chen et al.* discloses a flash memory comprising an array of non-volatile memory cells, a clock signal connection, data connections, a Rambus DRAM

interconnect configuration coupled to the array of memory cells, and output circuitry to provide output data on the data connections on both rising and falling edges of the clock signal. However, *Chen et al.* does not disclose a flash memory that has Rambus-compatible interconnections and circuitry to provide input and output data on rising and falling edges of a clock as claimed in the present application. The flash memory device disclosed in *Chen et al.* is briefly mentioned only in reference to typical memory devices and no detail is provided as to any flash memory functionality combined with a Rambus proprietary interconnect configuration and double data rate data connections.

There is also no suggestion or motivation in *Chen et al.* to combine the disclosure of the Rambus DRAM with the briefly mentioned flash memory device, even if they are disclosed in the same reference. The advantages of the input/output interface of *Chen et al.*, as discussed in the previous section, are to allow for high speed/bandwidth memory accesses while reducing the pin count and operating frequency of a memory IC. Combining a Rambus proprietary interconnect configuration with non-volatile memory cells, as is claimed in the Appellants' claims, does not achieve any of the advantages expressed in *Chen et al.* As is discussed in Appellants' specification (i.e., page 6, paragraph 22), the combination of a Rambus proprietary interconnection to non-volatile memory cells allows both volatile and non-volatile memory devices to use a unified communication bus.

With reference to the independent claims of the instant application, one element of apparatus claims 1, 4, and 18 is to "a rambus dynamic random access memory (RDRAM) interconnect configuration coupled to the array of non-volatile memory cells, the interconnect configuration comprising a multiplexed row address bus, a multiplexed column address bus, and data connections that are burst oriented." As discussed above, there is no suggestion or motivation in *Chen et al.* to combine the disclosure of the Rambus DRAM and the mention of the flash memory.

D. A Prima Facie Case of Obviousness Has Not Been Made

As illustrated in the case law above in Section 9(A), one required element for a prima facie case of obviousness is that there must be some suggestion or motivation, either in the

references themselves or in the knowledge generally available to one of ordinary skill in the art, to combine the reference teachings. Further, the teaching or suggestion to make the claimed combination must be found in the prior art and not based on Appellant's disclosure.

It has been shown in the previous section that there is no suggestion or motivation found in either *Chen et al.* or *Deneroff et al.* to combine a Rambus interconnect configuration with a flash memory array, as is claimed in the Appellants' amended claims. Therefore, the Examiner has not made a prima facie case of obviousness.

E. The Dependent Claims Are Also Allowable

If an independent claim is nonobvious under 35 U.S.C. §103, then any claim depending therefrom is nonobvious. *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988). Thus, for all the reasons stated above with respect to independent claims #'s 1, 4, and 18, the dependent claims are also allowable.

10. Conclusion

Appellants have set forth reasons why the Examiner is incorrect in maintaining his rejection of the pending claims. Appellants respectfully submit that, for the above reasons, claims 1 – 4 and 14 – 19 are allowable over the cited art, either alone or in combination. Therefore, reversal of the Examiner's rejection is respectfully requested.

Respectfully submitted,

Date: 9/8/03

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APPENDIX A

Claims on Appeal

1. A flash memory comprising:

an array of non-volatile memory cells;

a clock signal connection to receive a clock signal;

a rambus dynamic random access memory (RDRAM) interconnect configuration coupled to the array of non-volatile memory cells, the interconnect configuration comprising a multiplexed row address bus, a multiplexed column address bus, and data connections that are burst oriented; and

output circuitry to provide output data on the data connections on rising and falling edges of the clock signal.

2. The flash memory of claim 1 further comprising sense amplifier circuitry coupled to the array, wherein the sense amplifier circuitry detects a differential voltage.

3. The flash memory of claim 1 further comprising input circuitry to receive input data on the data connections on rising and falling edges of a the clock signal.

4. A flash memory comprising:

an array of non-volatile memory cells;

a clock signal connection to receive a clock signal;

a rambus dynamic random access memory (RDRAM) interconnect configuration coupled to the array of non-volatile memory cells, the interconnect configuration comprising a

multiplexed row address bus, a multiplexed column address bus, and data connections that are burst oriented;

output circuitry to provide output data on the data connections on rising and falling edges of the clock signal; and

input circuitry to receive input data on the data connections on rising and falling edges of the clock signal.

14. The flash memory of claim 1, wherein the array of non-volatile memory cells are arranged in a plurality of addressable banks.

15. The flash memory of claim 14, wherein each addressable bank contains addressable sectors of memory cells.

16. The flash memory of claim 1, wherein the output circuitry is adapted to provide the output data starting at a selected location and continuing for a programmed number of locations in a programmed sequence.

17. The flash memory of claim 4, wherein the output circuitry is further adapted to provide the output data starting at a selected location and continuing for a programmed number of locations in a programmed sequence.

18. A flash memory comprising:

an array of non-volatile memory cells arranged in a plurality of addressable banks;

a clock signal connection to receive a clock signal;

a rambus dynamic random access memory (RDRAM) interconnect configuration coupled to the array of non-volatile memory cells, the interconnect configuration comprising a multiplexed row address bus, a multiplexed column address bus, and data connections that are burst oriented;

output circuitry to provide output data on the data connections on rising and falling edges of the clock signal;

input circuitry to receive input data on the data connections at a rate of two data words per clock cycle; and

sense amplifier circuitry coupled to the array, wherein the sense amplifier circuitry detects a differential voltage.

19. The flash memory of claim 18, wherein the memory is adapted to provide burst-oriented read accesses.

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Enclosures

The following documents are enclosed:

X An Appeal Brief in triplicate includes Title Page and Table of Contents (1 pg.); Brief (pgs. 2-7); Appendix A (pgs. 8-10) (10 pgs. total)

X A check in the amount of $320.00 for the Appeal Brief Fee.

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